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APPL-DATE: November 11, 1996

INT-CL (IPC): H01L029/866;H01L029/78

ABSTRACT:

PROBLEM TO BE SOLVED: To increase the circumference and area, reduce the internal resistance, and enhance the electrostatic strength of, a Zener diode by forming the Zener diode for gate protection along the periphery of a chip, so that its cell region will be encircled.

SOLUTION: Polysilicon Zeners 9 are formed along the periphery of a chip 21, so that its cell region 10 will be encircled. The polysilicon Zeners 9 are alternately formed in the direction in which an n<SP>+</SP>-type polysilicon 12, where p-type ion seeds are implanted in polysilicon connects the central portion and peripheral portion of the chip 21 to constitute a kind of Zener diode. The polysilicon Zeners 9 are formed on a silicon substrate 13 with a gate oxide film 14 in-between, and the n<SP>+</SP>-type polysilicon 12 closest to the center of the chip is connected with the source of a transistor through the source Al electrode 16 on the layer-insulating film 15. Thereby the area of the polysilicon Zeners 9 is increased and the internal resistance can be

reduced.

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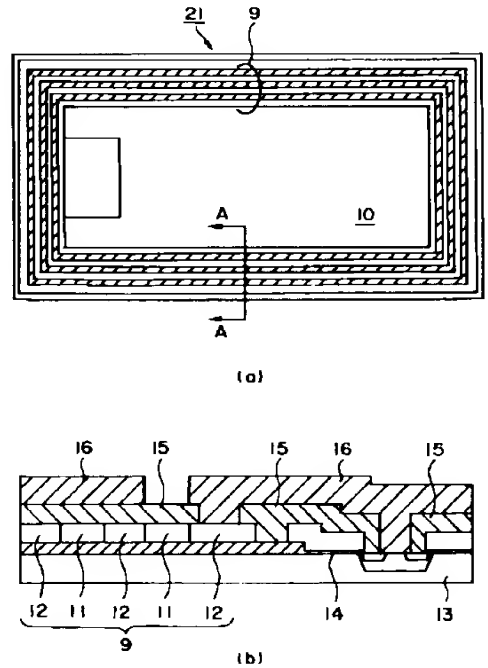
(54)【発明の名称】　半導体装置

(57)【要約】

【課題】　ポリシリツェナーの内部抵抗を低減することで静電耐量を向上させ、ゲート保護能力の高いポリシリツェナーを備えた半導体装置を提供する。

【解決手段】　ポリシリツェナー９がセル領域１０を囲むようにチップ２１の外周部に沿って形成されたことで従来に比べて面積が大きくなっている。このポリシリツェナー９は、ポリシリコン中にｐ型イオン種が導入されたＰ型ポリシリコン１１、ｎ型イオン種が導入されたＮ＋型ポリシリコン１２がチップ２１の中央部と外周部を結ぶ方向に交互に形成されたものである。



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【特許請求の範囲】

【請求項１】　Ｐ型領域とＮ型領域がチップの中央部と外周部を結ぶ方向に交互に形成されたポリシリコンからなるゲート保護用ツェナーダイオードが、セル領域を囲むようにチップの外周部に沿って形成されたことを特徴とする半導体装置。

【請求項２】　請求項１に記載の半導体装置において、前記ゲート保護用ツェナーダイオードが前記チップの外周部に加えてゲートパッドも囲むように形成されたことを特徴とする半導体装置。

【請求項３】　請求項１または２に記載の半導体装置において、

前記ゲート保護用ツェナーダイオードを構成するポリシリコンのＰ型領域、Ｎ型領域各々の寸法を調節することにより前記ゲート保護用ツェナーダイオードの耐圧を制御することを特徴とする半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置に関し、特にゲート保護デバイスとしてのツェナーダイオードを備えた半導体装置に関するものである。

【０００２】

【従来の技術】通常、半導体装置におけるトランジスタのゲートは、ゲート－基板間のキャパシタの誘電体を構成するシリコン酸化膜によってデバイスの残りの部分と隔てられている。ところが、あまりにも高い電圧がゲートに印加されると、誘電体のブレークダウン電界強度を超えてしまい、シリコン酸化膜が破壊され、ゲートと基板が短絡してデバイスが永久に破壊されることになる。また、ＭＯＳゲートキャパシタは寸法が小さく、品質が高いので、ゲートは浮遊静電荷による損傷を極めて受けやすい。そこで、この静電荷からゲートを保護する手段の一つとして、ゲートに種々の保護デバイスを接続するという方法がある。その一つの例を図７に示す。

【０００３】図７に示すように、トランジスタ１のゲートＧ－ソースＳ間に保護デバイスとしてゲートポリシリコンを用いて形成したツェナーダイオード２（以下、ポリシリツェナーと略称する）を接続する。この際、ポリシリツェナー２の耐圧がゲートＧ－ソースＳ間破壊耐圧より小さくなるように設計しておく。このような構造とすれば、ゲートＧ－ソースＳ間に静電気による過電圧が印加された場合でも、ゲートＧ－ソースＳ間の電圧がゲート－ソース間破壊耐圧に至る前にポリシリツェナー２の方がブレークダウンするため、トランジスタの破壊が防止される。

【０００４】図８は従来一般のポリシリツェナーの配置を示す図である。この図に示すように、チップ３内において、Ｐ型領域４とＮ型領域５が交互に配置されたポリシリツェナー２はトランジスタのゲートの端子部であるゲートパッド６を囲むような形状でパッド形成領域７内

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のゲートパッド６の周囲にのみ形成されるのが通常であった。

【０００５】

【発明が解決しようとする課題】しかしながら、上記従来のポリシリツェナーを備えた半導体装置においては、チップが縮小化すればするほど静電耐量（静電荷に対する破壊耐圧）も小さくなるため、トランジスタが破壊されやすくなるという問題点があった。その理由は、静電耐量を向上させるためにはポリシリツェナーの内部抵抗を小さくしてポリシリツェナー側に電荷を逃がしやすくすることが重要な要因である。一方、チップの有効セル面積を確保するために、通常、ゲートパッドはワイヤボンディングができる程度に極力小さくするものである。また、チップが小さくなれば必然的にゲートパッドも小さくなる。ところが、ポリシリツェナーを形成できる領域の面積がゲートパッドの寸法に依存するため、ゲートパッドが小さくなるとポリシリツェナーの形成領域も小さくなる。すると、ポリシリツェナーの内部抵抗が結果的に大きくなるため、静電耐量が小さくなるからである。

【０００６】本発明は、上記の課題を解決するためになされたものであって、ポリシリツェナーの内部抵抗を低減することで従来に比べて静電耐量を向上させ、ゲート保護能力の高いポリシリツェナーを備えた半導体装置を提供することを目的とする。

【０００７】

【課題を解決するための手段】上記の目的を達成するために、本発明の請求項１に記載の半導体装置は、Ｐ型領域とＮ型領域がチップの中央部と外周部を結ぶ方向に交互に形成されたポリシリコンからなるゲート保護用ツェナーダイオードが、セル領域を囲むようにチップの外周部に沿って形成されたことを特徴とするものである。

【０００８】また、請求項２に記載の半導体装置は、前記ゲート保護用ツェナーダイオードが前記チップの外周部に加えてゲートパッドも囲むように形成されたことを特徴とするものである。

【０００９】また、請求項３に記載の半導体装置は、前記ゲート保護用ツェナーダイオードを構成するポリシリコンのＰ型領域、Ｎ型領域各々の寸法を調節することにより前記ゲート保護用ツェナーダイオードの耐圧を制御することを特徴とするものである。

【００１０】本発明の半導体装置においては、ゲート保護用ツェナーダイオードをセル領域を囲むようにチップの外周部に沿って形成したことによってゲートパッドの周囲のみを囲むように形成した従来の場合に比べてツェナーダイオードの周長が長くなる。その結果、ツェナーダイオードの面積が大きくなり、内部抵抗を小さくできることによって静電耐量を向上させることが可能になる。

【００１１】

【発明の実施の形態】以下、本発明の一実施の形態を図１～図３を参照して説明する。図１（ａ）は本実施の形態の半導体装置の全体構成を示す平面図、図１（ｂ）は断面図であり、本実施の形態の半導体装置も従来技術の項で述べたものと同様、トランジスタのゲート－ソース間にゲート保護デバイスとしてポリシリツェナー（ゲート保護用ツェナーダイオード）を接続したものである。

【００１２】図１（ａ）に示すように、本実施の形態の半導体装置の場合、ポリシリツェナー９がセル領域１０を囲むようにチップ２１の外周部に沿って形成されている。また、図１（ｂ）に示すように、ポリシリツェナー９はポリシリコン中にｐ型イオン種が導入されたＰ型ポリシリコン１１（Ｐ型領域）、ｎ型イオン種が導入されたN^+型ポリシリコン１２（Ｎ型領域）がチップ２１の中央部と外周部を結ぶ方向に交互に形成されて一種のツェナーダイオードを構成するものである。そして、シリコン基板１３上にゲート酸化膜１４を介してポリシリツェナー９が形成され、その最もチップ中央側のN^+型ポリシリコン１２は層間絶縁膜１５上のソースＡｌ電極１６を介してトランジスタのソース（図示略）と接続されている。

【００１３】次に、図２を用いて上記構成のポリシリツェナー９を形成する手順について説明する。図２は、上記半導体装置をチップ２１の中央部と外周部を結ぶ方向に沿って切断した状態を示す断面図である。まず、図２（ａ）に示すように、シリコン基板１３上にゲート酸化膜１４を形成し、さらに後でポリシリツェナーとなるノンドープポリシリコン１７を形成する。そして、フォトリソグラフィー・エッチング技術を用いてノンドープポリシリコン１７を所望の形状、寸法にパターニングする。次に、ポリシリツェナーを形成するための基盤としてノンドープポリシリコン１７全体を一旦Ｐ型ポリシリコン１１とする。すなわち、図２（ｂ）に示すように、セル領域をフォトレジスト１８でマスクした後、イオン注入技術を用いて^{11}B、$^{49}BF_2$等のＰ型イオン種をポリシリツェナー形成領域のノンドープポリシリコン１７中に導入する。

【００１４】次に、図２（ｃ）に示すように、セル領域のＮ型領域１９およびポリシリツェナー９のＮ型高濃度領域を形成するために、フォトリソグラフィー技術を用いてこれらの領域が開口したフォトレジスト１８を形成する。その後、イオン注入技術を用いて^{31}P、^{75}As等のN^+型イオン種をセル領域においてはシリコン基板１３中に、ポリシリツェナー形成領域においてはＰ型ポリシリコン１１中に高濃度で導入する。すると、ポリシリツェナー形成領域ではＰ型ポリシリコン１１のフォトレジスト１８に覆われていない部分がN^+型に反転することでＰ型ポリシリコン１１とN^+型ポリシリコン１２が交互に形成された状態となる。最後に、フォトレジスト１８を除去した後、図２（ｄ）に示すように、各領域のポリシリコンを覆う層間絶縁膜１５、ソースＡｌ電極１６を形成することによってポリシリツェナー９が形成される。

【００１５】本実施の形態の半導体装置においては、ポリシリツェナー９をセル領域１０を囲むようにチップ２１の外周部に沿って形成したことによってゲートパッドの周囲を囲むように形成した従来の場合に比べてポリシリツェナー９の周長が長くなる。したがって、ポリシリツェナー９の面積が従来に比べて大きくなり、内部抵抗を小さくできるため、静電耐量を向上させることが可能になる。

【００１６】図３はポリシリツェナーのＩ－Ｖ特性を示す概念図であるが、この図に示すように、本実施の形態の場合、内部抵抗が小さくなったことでポリシリツェナーがブレークダウンした後のＩ－Ｖ特性曲線の勾配が従来に比べて大きくなっている。セル領域のゲート酸化膜の絶縁耐圧をV_Bとすると、V_Bという同じ電圧が印加された場合でも、本実施例のポリシリツェナーでは従来のものに比べてダイオードを流れる電流が大きくなることがわかる。すなわち、ゲート－ソース間の静電荷がポリシリツェナーを通じて逃げやすくなり、従来に比べて静電耐量が向上する。

【００１７】一例として、チップサイズ３ｍｍ×３ｍｍ程度のデバイスを考えた場合、ゲート酸化膜厚を５００Åとすると、ポリシリツェナーをゲートパッドの周囲に形成した従来の半導体装置ではポリシリツェナーの面積が$2\times10^{-3}mm^2$、内部抵抗が３５Ωとなり、ツェナーダイオードの耐圧（以下、ツェナー耐圧と称する）を２５～３０Ｖとすると、静電耐量はＭＩＬ法で２５００～３０００Ｖとなる。それに対して、ポリシリツェナー９をチップ外周部に形成した本実施の形態の場合、ツェナー耐圧自体は２５～３０Ｖと変わらないが、ポリシリツェナー９の面積が約$12\times10^{-3}mm^2$に増えることで内部抵抗が約６Ωに低減するため、静電耐量は３０００～４０００Ｖに増大し、従来に比べて１．２～１．４倍程度向上する。

【００１８】また、本実施の形態の半導体装置の場合、従来と比べてポリシリツェナー９のレイアウトを変えるだけであって、ポリシリツェナー９の構造やセル領域等、他の部分には全く変更がないため、製造プロセスを変更することなく静電耐量向上という上記の利点を得ることができる。

【００１９】次に、上記実施の形態の変形例として、図４に示すように、ポリシリツェナー２２をチップ２１の外周部に加えてゲートパッド２３も一部囲むように形成した構造としてもよい。このような構造にすると、ポリシリツェナー２２の周長（面積）をより大きくすることができ、内部抵抗の低減によって静電耐量をさらに向上させることが可能になる。

【００２０】さらに、ポリシリツェナーの構成として、

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図5に示すように、P型ポリシリコン11、N+型ポリシリコン12の位置関係を上記実施の形態と逆にすることも可能である。また、上述した具体例ではツェナー耐圧自体は従来と変わらないものとしたが、図6に示すように、P型ポリシリコン11、N+型ポリシリコン12の寸法を適宜変化させることによってツェナー耐圧そのものを調節し、静電耐量をコントロールすることもできる。

【0021】

【発明の効果】以上、詳細に説明したように、本発明の半導体装置によれば、ゲート保護用ツェナーダイオードをセル領域を囲むようにチップの外周部に沿って形成したことによって従来の場合に比べてツェナーダイオードの周長が長くなる。その結果、ツェナーダイオードの面積が従来に比べて大きくなり、内部抵抗が小さくなるため、静電耐量を向上させることが可能になる。したがって、ゲート保護能力の高いツェナーダイオードを備えた半導体装置を提供することができる。また、本発明では、ゲート保護用ツェナーダイオードのレイアウトを従来と変えるだけであり、ツェナーダイオードの構造やセル領域等には全く変更がないため、製造プロセスを変更することなく静電耐量向上という上記の利点を得ることができる。

【図面の簡単な説明】

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【図1】　本発明の一実施の形態であるポリシリツェナーを備えた半導体装置を示す、（a）平面図、（b）（a）のA－A線に沿う断面図である。

【図2】　同ポリシリツェナーの形成方法を示すプロセスフロー図である。

【図3】　従来と本実施の形態のポリシリツェナーのI－V特性を示す概念図である。

【図4】　本実施の形態のポリシリツェナーの変形例を示す平面図である。

【図5】　他の変形例を示す断面図である。

【図6】　さらに他の変形例を示す断面図である。

【図7】　ツェナーダイオードを用いたゲート保護の一例を示す概念図である。

【図8】　ポリシリツェナーを備えた従来の半導体装置の一例を示す平面図である。

【符号の説明】

9，22　ポリシリツェナー（ゲート保護用ツェナーダイオード）

10　セル領域

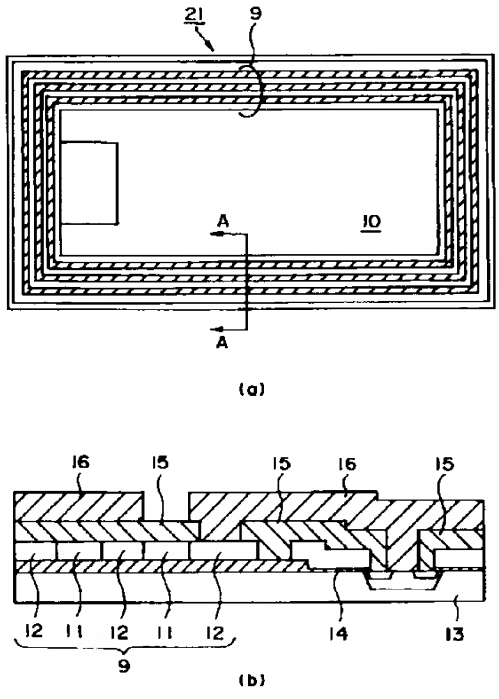
11　P型ポリシリコン（P型領域）

12　N+型ポリシリコン（N型領域）

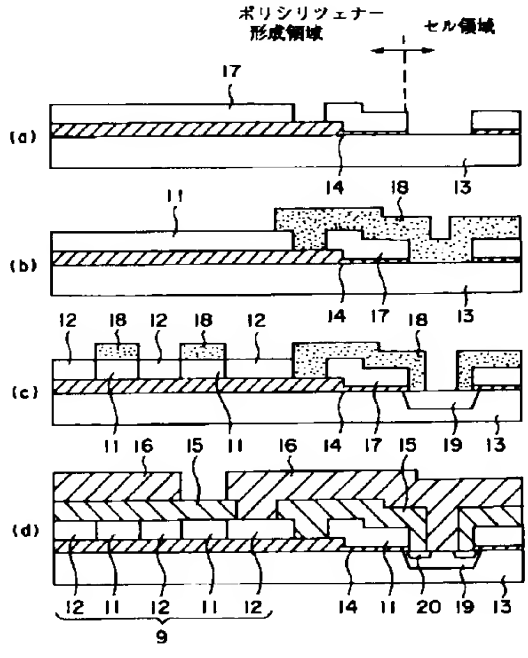
21　チップ

23　ゲートパッド

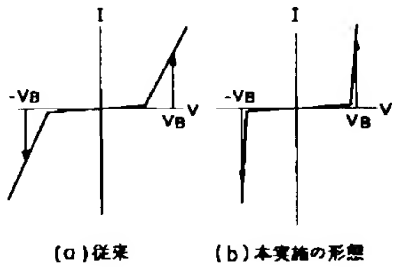
【図1】



【図2】

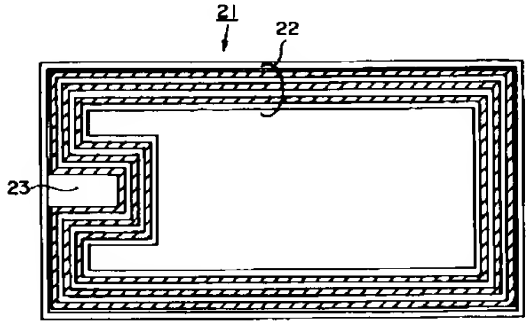


【図3】

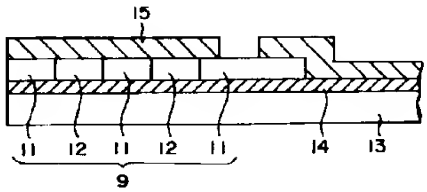


(a)従来　　(b)本実施の形態

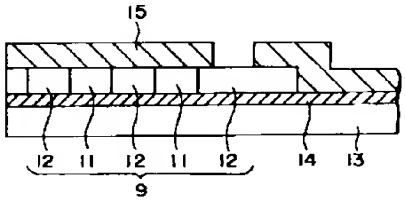
【図4】



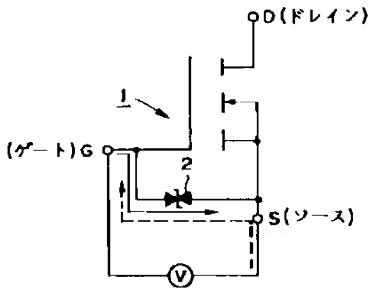
【図5】



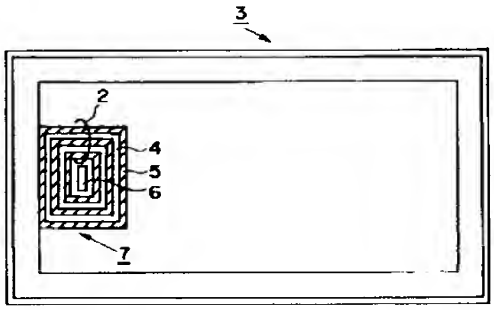
【図6】



【図7】



【図8】



DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device equipped with the zener diode as a gate protection device about a semiconductor device.
[0002]
[Description of the Prior Art] Usually, the gate of the transistor in a semiconductor device is separated from the remaining portion of a device by the silicon oxide which constitutes the dielectric of the capacitor between gate-substrates. However, when too much high voltage is impressed to the gate, the breakdown field strength of a dielectric is exceeded, a silicon oxide is destroyed, the gate and a substrate will short-circuit and a device will be destroyed eternally. Moreover, since an MOS gate capacitor has a small size and quality is high, the gate tends [very] to receive the injury by suspension electrostatic charge. Then, the method of connecting various protection devices is in the gate as one of the meanses which protects the gate from this electrostatic charge. The one example is shown in drawing 7 .
[0003] As shown in drawing 7 , the zener diode 2 (it is hereafter called a polysilicon Zener for short) which used and formed contest gate polysilicon as a protection device between the gate G-sources S of a transistor 1 is connected. Under the present circumstances, it designs so that pressure-proofing of polysilicon Zener 2 may become smaller than the gate G-source S destructive pressure-proofing. Destruction of a transistor is prevented in order that the direction of polysilicon Zener 2 may carry out breakdown before the voltage between the gate G-sources S results in gate-source destructive pressure-proofing, even when the overvoltage by static electricity is impressed between such structure, then the gate G-source S.
[0004] Drawing 8 is drawing showing arrangement of the polysilicon Zener of the general former. As shown in this drawing, usually polysilicon Zener 2 by which the P type field 4 and the N type field 5 have been arranged by turns in a chip 3 was formed only in the circumference of the gate pad 6 in the pad formation field 7 in a configuration which surrounds the gate pad 6 which is the terminal area of the gate of a transistor.
[0005]
[Problem(s) to be Solved by the Invention] However, in the semiconductor device equipped with the above-mentioned conventional polysilicon Zener, since the electrostatic tolerance dose (destructive proof pressure to electrostatic charge) also became smaller as a chip reduction-izes, there was a trouble that a transistor became is easy to be destroyed. In order to raise the electrostatic tolerance dose, the reason makes internal resistance of a polysilicon Zener small, and is a factor with important for a polysilicon Zener side making a charge easy to miss. On the other hand, in order to secure the effective cell area of a chip, a gate pad is usually made small as much as possible at the grade which can do wirebonding. Moreover, if a chip becomes small, a gate pad will also become small inevitably. However, in order that the area of the field which can form a polysilicon Zener may be dependent on the size of a gate pad, if a gate pad becomes small, the formation field of a polysilicon Zener will also become small. Then, it is because the electrostatic tolerance dose becomes small since the internal resistance of a polysilicon Zener becomes large as a result.
[0006] this invention is made in order to solve the above-mentioned technical problem, it raises the electrostatic tolerance dose compared with the former by reducing the internal resistance of a polysilicon Zener, and aims at offering the semiconductor device equipped with the high polysilicon Zener of gate protection capacity.
[0007]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device of this invention according to claim 1 is characterized by forming the zener diode for gate protection which a P type field and an N type field become from contest polysilicon formed in the direction to which the center section and the periphery section of a chip are connected by turns along with the periphery section of a chip so that a cell field may be surrounded.
[0008] Moreover, a semiconductor device according to claim 2 is characterized by being formed so that the aforementioned zener diode for gate protection may also surround a gate pad in addition to the periphery section of the aforementioned chip.
[0009] moreover, a semiconductor device according to claim 3 is characterized by controlling pressure-proofing of the aforementioned zener diode for gate protection by adjusting the P type field of contest polysilicon which constitutes the aforementioned zener diode for gate protection, and the size of each N type field
[0010] In the semiconductor device of this invention, the circumference of zener diode becomes long compared with the case of the former formed so that only the circumference of a gate pad might be surrounded by having formed the zener diode for

gate protection along with the periphery section of a chip so that a cell field might be surrounded. Consequently, the area of zener diode becomes large and it becomes possible by the ability making internal resistance small to raise the electrostatic tolerance dose.

[0011]

[Embodiments of the Invention] Hereafter, the gestalt of 1 operation of this invention is explained with reference to drawing 1 - drawing 3 . Drawing 1 (a) connects a polysilicon Zener (zener diode for gate protection) as a gate protection device between the gate-sources of a transistor like [the plan and drawing 1 (b) which show the whole semiconductor device composition of the gestalt of this operation are a cross section, and] what also stated the semiconductor device of the gestalt of this operation by the term of the conventional technology.

[0012] As shown in drawing 1 (a), in the case of the semiconductor device of the gestalt of this operation, along with the periphery section of a chip 21, it is formed so that polysilicon Zener 9 may surround the cell field 10. Moreover, polysilicon Zener 9 is N+ into which contest 11 (P type field) P type polysilicon with which p type ion kind was introduced into the polysilicon contest as shown in drawing 1 (b), and n type ion kind were introduced. Contest 12 (N type field) type polysilicon is formed in the direction to which the center section and the periphery section of a chip 21 are connected by turns, and constitutes a kind of zener diode. and polysilicon Zener 9 forms through the gate oxide film 14 on a silicon substrate 13 -- having -- the -- most -- N+ of a chip central site Contest 12 type polysilicon is connected with the source (illustration abbreviation) of a transistor through the source aluminum electrode 16 on the layer insulation film 15.

[0013] Next, the procedure which forms polysilicon Zener 9 of the above-mentioned composition using drawing 2 is explained. Drawing 2 is the cross section showing the state where the above-mentioned semiconductor device was cut along the direction to which the center section and the periphery section of a chip 21 are connected. First, as shown in drawing 2 (a), the gate oxide film 14 is formed on a silicon substrate 13, and contest 17 non dope polysilicon which becomes a polysilicon Zener further later is formed. And patterning of contest 17 non dope polysilicon is carried out to a desired configuration and a size using photo lithography etching technology. Next, the non dope polysilicon contest 17 whole is once considered as contest 11 P type polysilicon as a base for forming a polysilicon Zener. namely, the ion-implantation technology as shown in drawing 2 (b), after carrying out the mask of the cell field by the photoresist 18 -- using -- 11B and 49BF2 etc. -- a P type ion kind is introduced into contest 17 non dope polysilicon of a polysilicon Zener formation field

[0014] Next, as shown in drawing 2 (c), in order to form the N type field 19 of a cell field, and the N type high concentration field of polysilicon Zener 9. the photoresist 18 in which used photo lithography technology and these fields carried out opening is formed. Then, ion-implantation technology is used and they are N+, such as 31P and 75As. A type ion kind is introduced by high concentration into contest 11 P type polysilicon in a polysilicon Zener formation field into a silicon substrate 13 in a cell field. Then, the portion which is not covered by the photoresist 18 of contest 11 P type polysilicon in a polysilicon Zener formation field is N+. They are contest 11 P type polysilicon and N+ by it being reversed to type. Contest 12 type polysilicon will be in the state where it was formed by turns. Finally, after removing a photoresist 18, as shown in drawing 2 (d), polysilicon Zener 9 is formed in contest polysilicon of each field by forming the wrap layer insulation film 15 and the source aluminum electrode 16.

[0015] In the semiconductor device of the gestalt of this operation, the circumference of polysilicon Zener 9 becomes long compared with the case of the former formed so that the circumference of a gate pad might be surrounded by having formed polysilicon Zener 9 along with the periphery section of a chip 21 so that the cell field 10 might be surrounded. Therefore, since the area of polysilicon Zener 9 becomes large compared with the former and can make internal resistance small, it becomes possible to raise the electrostatic tolerance dose.

[0016] Although drawing 3 is the conceptual diagram showing the I-V property of a polysilicon Zener, as shown in this drawing, in the case of the gestalt of this operation, the inclination of the I-V characteristic curve after a polysilicon Zener carries out breakdown because internal resistance became small is large compared with the former. It is VB about the isolation voltage of the gate oxide film of a cell field. It is VB if it carries out. Even when the same voltage to say is impressed, in the polysilicon Zener of this example, compared with the conventional thing, the flowing current is large and a bird clapper understands diode. That is, the electrostatic charge between the gate-sources becomes easy to escape through a polysilicon Zener, and the electrostatic tolerance dose improves compared with the former.

[0017] If gate oxidization thickness is made into 500A as an example when an about [chip size 3mmx3mm] device is considered With the conventional semiconductor device formed in the circumference of a gate pad, the area of a polysilicon Zener a polysilicon Zener 2x10 to 3 mm2, If internal resistance is set to 35 ohms and sets the proof pressure (Zener pressure-proofing is called hereafter) of zener diode to 25-30V, the electrostatic tolerance dose will be set to 2500-3000V by the MIL method. Although the Zener proof pressure itself does not change with 25-30V in the case of the gestalt of this operation which formed polysilicon Zener 9 in the chip periphery section to it, the area of polysilicon Zener 9 is about 12x10 to 3 mm2. In order that internal resistance may decrease to about 6 ohms by increasing, the electrostatic tolerance dose increases to 3000-4000V, and improves by about 1.2 to 1.4 times compared with the former.

[0018] Moreover, in the case of the semiconductor device of the form of this operation, compared with the former, the layout of polysilicon Zener 9 is only changed, and since there is no change in other portions, structure, a cell field, etc. of polysilicon Zener 9 can acquire the above-mentioned advantage of the improvement in electrostatic ****, without changing a manufacture process.

[0019] Next, as a modification of the gestalt of the above-mentioned implementation, as shown in drawing 4 , it is good also

as structure formed so that polysilicon Zener 22 might be added to the periphery section of a chip 21 and the gate pad 23 might also be surrounded in part. If it is made such structure, the circumference (area) of polysilicon Zener 22 can be enlarged more, and it will become possible to raise the electrostatic tolerance dose further by reduction of internal resistance.

[0020] Furthermore, as composition of a polysilicon Zener, as shown in drawing 5 , they are contest 11 P type polysilicon and N+. It is also possible to make physical relationship of contest 12 type polysilicon into the gestalt and reverse of the above-mentioned implementation. Moreover, although the Zener proof pressure itself shall not change with the former, as it is shown in drawing 6 by the example mentioned above, they are contest 11 P type polysilicon and N+. By changing the size of contest 12 type polysilicon suitably, the Zener proof pressure itself can be adjusted and the electrostatic tolerance dose can also be controlled.

[0021]

[Effect of the Invention] As mentioned above, as explained in detail, according to the semiconductor device of this invention, compared with the conventional case, the circumference of zener diode becomes long by having formed the zener diode for gate protection along with the periphery section of a chip so that a cell field might be surrounded. Consequently, since the area of zener diode becomes large compared with the former and internal resistance becomes small, it becomes possible to raise the electrostatic tolerance dose. Therefore, the semiconductor device equipped with the high zener diode of gate protection capacity can be offered. Moreover, in this invention, since the layout of the zener diode for gate protection is only changed with the former and there is no change in the structure and the cell field of zener diode, the above-mentioned advantage of the improvement in the electrostatic tolerance dose can be acquired, without changing a manufacture process.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device equipped
with the zener diode as a gate protection device about a semiconductor device.
[0002]
[Description of the Prior Art] Usually, the gate of the transistor in a semiconductor device is separated from the remaining
portion of a device by the silicon oxide which constitutes the dielectric of the capacitor between gate-substrates.
However, when too much high voltage is impressed to the gate, the breakdown field strength of a dielectric is exceeded, a
silicon oxide is destroyed, the gate and a substrate will short-circuit and a device will be destroyed eternally. Moreover,
since an MOS gate capacitor has a small size and quality is high, the gate tends [very] to receive the injury by
suspension electrostatic charge. Then, the method of connecting various protection devices is in the gate as one of the
meanses which protects the gate from this electrostatic charge. The one example is shown in drawing 7 .
[0003] As shown in drawing 7 , the zener diode 2 (it is hereafter called a polysilicon Zener for short) which used and
formed contest gate polysilicon as a protection device between the gate G-sources S of a transistor 1 is connected. Under
the present circumstances, it designs so that pressure-proofing of polysilicon Zener 2 may become smaller than the gate
G-source S destructive pressure-proofing. Destruction of a transistor is prevented in order that the direction of polysilicon
Zener 2 may carry out breakdown before the voltage between the gate G-sources S results in gate-source destructive
pressure-proofing, even when the overvoltage by static electricity is impressed between such structure, then the gate
G-source S.

[0004] Drawing 8 is drawing showing arrangement of the polysilicon Zener of the general former. As shown in this
drawing, usually polysilicon Zener 2 by which the P type field 4 and the N type field 5 have been arranged by turns in a
chip 3 was formed only in the circumference of the gate pad 6 in the pad formation field 7 in a configuration which
surrounds the gate pad 6 which is the terminal area of the gate of a transistor.
[0005]
[Problem(s) to be Solved by the Invention] However, in the semiconductor device equipped with the above-mentioned
conventional polysilicon Zener, since the electrostatic tolerance dose (destructive proof pressure to electrostatic charge)
also became smaller as a chip reduction-izes, there was a trouble that a transistor became is easy to be destroyed. In order
to raise the electrostatic tolerance dose, the reason makes internal resistance of a polysilicon Zener small, and is a factor
with important for a polysilicon Zener side making a charge easy to miss. On the other hand, in order to secure the
effective cell area of a chip, a gate pad is usually made small as much as possible at the grade which can do wirebonding.
Moreover, if a chip becomes small, a gate pad will also become small inevitably. However, in order that the area of the field
which can form a polysilicon Zener may be dependent on the size of a gate pad, if a gate pad becomes small, the formation
field of a polysilicon Zener will also become small. Then, it is because the electrostatic tolerance dose becomes small since
the internal resistance of a polysilicon Zener becomes large as a result.
[0006] this invention is made in order to solve the above-mentioned technical problem, it raises the electrostatic tolerance
dose compared with the former by reducing the internal resistance of a polysilicon Zener, and aims at offering the
semiconductor device equipped with the high polysilicon Zener of gate protection capacity.
[0007]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device of this
invention according to claim 1 is characterized by forming the zener diode for gate protection which a P type field and an N
type field become from contest polysilicon formed in the direction to which the center section and the periphery section of
a chip are connected by turns along with the periphery section of a chip so that a cell field may be surrounded.
[0008] Moreover, a semiconductor device according to claim 2 is characterized by being formed so that the aforementioned
zener diode for gate protection may also surround a gate pad in addition to the periphery section of the aforementioned

chip.
[0009] moreover, a semiconductor device according to claim 3 is characterized by controlling pressure-proofing of the
aforementioned zener diode for gate protection by adjusting the P type field of contest polysilicon which constitutes the
aforementioned zener diode for gate protection, and the size of each N type field
[0010] In the semiconductor device of this invention, the circumference of zener diode becomes long compared with the
case of the former formed so that only the circumference of a gate pad might be surrounded by having formed the zener
diode for gate protection along with the periphery section of a chip so that a cell field might be surrounded. Consequently,
the area of zener diode becomes large and it becomes possible by the ability making internal resistance small to raise the
electrostatic tolerance dose.
[0011]
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drawing 1 - drawing 3 . Drawing 1 (a) connects a polysilicon Zener (zener diode for gate protection) as a gate protection
device between the gate-sources of a transistor like [the plan and drawing 1 (b) which show the whole semiconductor
device composition of the gestalt of this operation are a cross section, and] what also stated the semiconductor device of
the gestalt of this operation by the term of the conventional technology.
[0012] As shown in drawing 1 (a), in the case of the semiconductor device of the gestalt of this operation, along with the
periphery section of a chip 21, it is formed so that polysilicon Zener 9 may surround the cell field 10. Moreover, polysilicon
Zener 9 is N+ into which contest 11 (P type field) P type polysilicon with which p type ion kind was introduced into the
polysilicon contest as shown in drawing 1 (b), and n type ion kind were introduced. Contest 12 (N type field) type
polysilicon is formed in the direction to which the center section and the periphery section of a chip 21 are connected by
turns, and constitutes a kind of zener diode. and polysilicon Zener 9 forms through the gate oxide film 14 on a silicon
substrate 13 -- having -- the -- most -- N+ of a chip central site Contest 12 type polysilicon is connected with the source
(illustration abbreviation) of a transistor through the source aluminum electrode 16 on the layer insulation film 15.
[0013] Next, the procedure which forms polysilicon Zener 9 of the above-mentioned composition using drawing 2 is
explained. Drawing 2 is the cross section showing the state where the above-mentioned semiconductor device was cut

along the direction to which the center section and the periphery section of a chip 21 are connected. First, as shown in
drawing 2 (a), the gate oxide film 14 is formed on a silicon substrate 13, and contest 17 non dope polysilicon which
becomes a polysilicon Zener further later is formed. And patterning of contest 17 non dope polysilicon is carried out to a
desired configuration and a size using photo lithography etching technology. Next, the non dope polysilicon contest 17
whole is once considered as contest 11 P type polysilicon as a base for forming a polysilicon Zener, namely, the
ion-implantation technology as shown in drawing 2 (b), after carrying out the mask of the cell field by the photoresist 18 --
using -- 11B and 49BF2 etc. -- a P type ion kind is introduced into contest 17 non dope polysilicon of a polysilicon Zener
formation field
[0014] Next, as shown in drawing 2 (c), in order to form the N type field 19 of a cell field, and the N type high concentration
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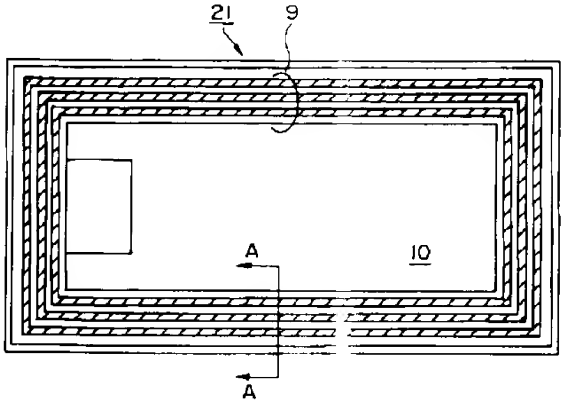
opening is formed. Then, ion-implantation technology is used and they are N+, such as 31P and 75As. A type ion kind is
introduced by high concentration into contest 11 P type polysilicon in a polysilicon Zener formation field into a silicon
substrate 13 in a cell field. Then, the portion which is not covered by the photoresist 18 of contest 11 P type polysilicon in
a polysilicon Zener formation field is N+. They are contest 11 P type polysilicon and N+ by it being reversed to type.
Contest 12 type polysilicon will be in the state where it was formed by turns. Finally, after removing a photoresist 18, as
shown in drawing 2 (d), polysilicon Zener 9 is formed in contest polysilicon of each field by forming the wrap layer
insulation film 15 and the source aluminum electrode 16.
[0015] In the semiconductor device of the gestalt of this operation, the circumference of polysilicon Zener 9 becomes long
compared with the case of the former formed so that the circumference of a gate pad might be surrounded by having
formed polysilicon Zener 9 along with the periphery section of a chip 21 so that the cell field 10 might be surrounded.
Therefore, since the area of polysilicon Zener 9 becomes large compared with the former and can make internal resistance
small, it becomes possible to raise the electrostatic tolerance dose.
[0016] Although drawing 3 is the conceptual diagram showing the I-V property of a polysilicon Zener, as shown in this
drawing, in the case of the gestalt of this operation, the inclination of the I-V characteristic curve after a polysilicon Zener

carries out breakdown because internal resistance became small is large compared with the former. It is VB about the
isolation voltage of the gate oxide film of a cell field. It is VB if it carries out. Even when the same voltage to say is
impressed. in the polysilicon Zener of this example, compared with the conventional thing, the flowing current is large and
a bird clapper understands diode. That is, the electrostatic charge between the gate-sources becomes easy to escape
through a polysilicon Zener, and the electrostatic tolerance dose improves compared with the former.
[0017] If gate oxidization thickness is made into 500A as an example when an about [chip size 3mmx3mm] device is
considered With the conventional semiconductor device formed in the circumference of a gate pad, the area of a
polysilicon Zener a polysilicon Zener 2x10 to 3 mm2, If internal resistance is set to 35 ohms and sets the proof pressure
(Zener pressure-proofing is called hereafter) of zener diode to 25-30V, the electrostatic tolerance dose will be set to
2500-3000V by the MIL method. Although the Zener proof pressure itself does not change with 25-30V in the case of the
gestalt of this operation which formed polysilicon Zener 9 in the chip periphery section to it, the area of polysilicon Zener
9 is about 12x10 to 3 mm2. In order that internal resistance may decrease to about 6 ohms by increasing. the electrostatic
tolerance dose increases to 3000-4000V, and improves by about 1.2 to 1.4 times compared with the former.
[0018] Moreover. in the case of the semiconductor device of the form of this operation, compared with the former, the
layout of polysilicon Zener 9 is only changed, and since there is no change in other portions, structure. a cell field, etc. of
polysilicon Zener 9 can acquire the above-mentioned advantage of the improvement in electrostatic ****. without
changing a manufacture process.
[0019] Next, as a modification of the gestalt of the above-mentioned implementation, as shown in drawing 4 . it is good
also as structure formed so that polysilicon Zener 22 might be added to the periphery section of a chip 21 and the gate pad
23 might also be surrounded in part. If it is made such structure, the circumference (area) of polysilicon Zener 22 can be
enlarged more. and it will become possible to raise the electrostatic tolerance dose further by reduction of internal
resistance.
[0020] Furthermore. as composition of a polysilicon Zener, as shown in drawing 5 , they are contest 11 P type polysilicon
and N+. It is also possible to make physical relationship of contest 12 type polysilicon into the gestalt and reverse of the

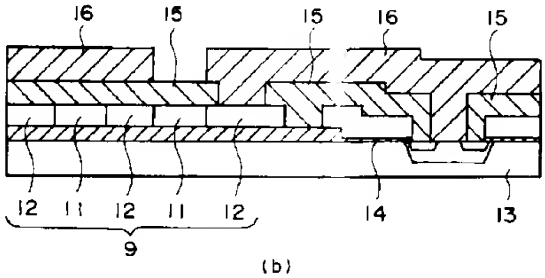
above-mentioned implementation. Moreover, although the Zener proof pressure itself shall not change with the former, as
it is shown in drawing 6 by the example mentioned above, they are contest 11 P type polysilicon and N+. By changing the
size of contest 12 type polysilicon suitably, the Zener proof pressure itself can be adjusted and the electrostatic tolerance
dose can also be controlled.
[0021]
[Effect of the Invention] As mentioned above, as explained in detail, according to the semiconductor device of this
invention, compared with the conventional case, the circumference of zener diode becomes long by having formed the
zener diode for gate protection along with the periphery section of a chip so that a cell field might be surrounded.
Consequently, since the area of zener diode becomes large compared with the former and internal resistance becomes
small, it becomes possible to raise the electrostatic tolerance dose. Therefore, the semiconductor device equipped with the
high zener diode of gate protection capacity can be offered. Moreover, in this invention, since the layout of the zener
diode for gate protection is only changed with the former and there is no change in the structure and the cell field of zener
diode, the above-mentioned advantage of the improvement in the electrostatic tolerance dose can be acquired, without
changing a manufacture process.

[Translation done.]

Drawing selection drawing 1



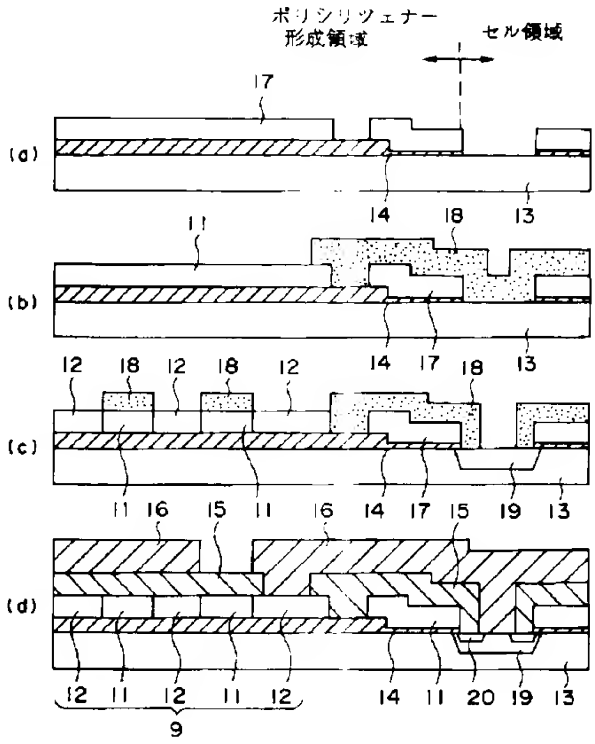
(a)



(b)

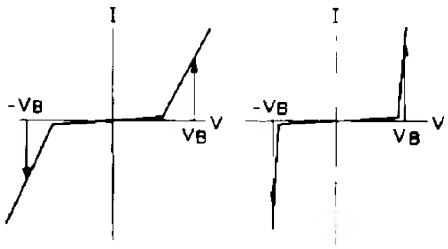
[Translation done.]

Drawing selection drawing 2



[Translation done.]

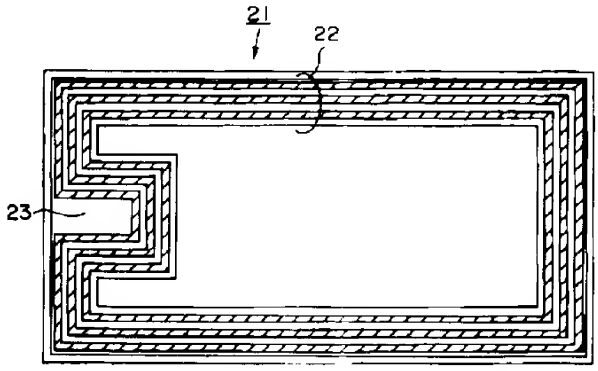
Drawing selection drawing 3



(a)従来　　(b)本実施の形態

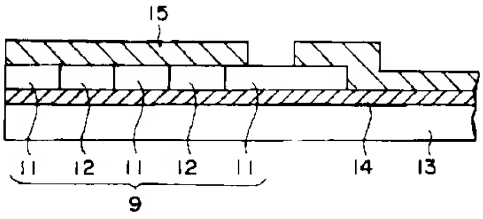
[Translation done.]

Drawing selection drawing 4



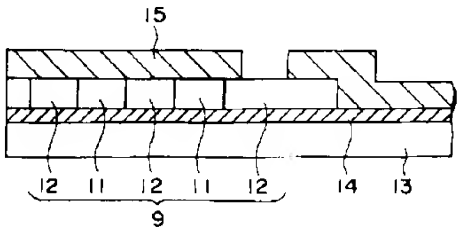
[Translation done.]

Drawing selection drawing 5



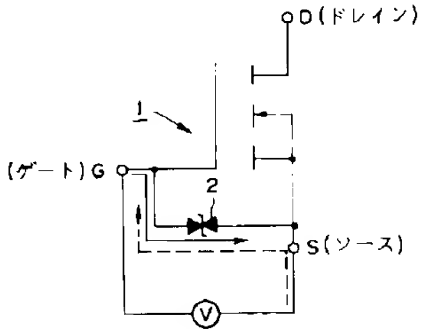
[Translation done.]

Drawing selection drawing 6



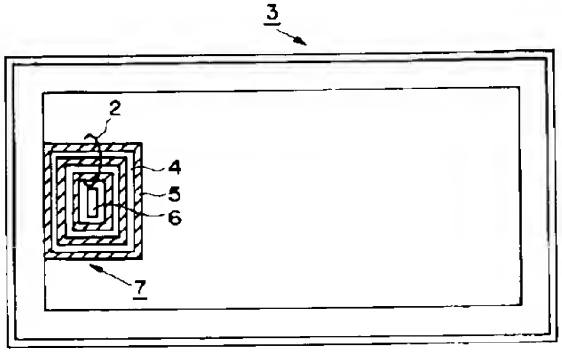
[Translation done.]

Drawing selection drawing 7



[Translation done.]

Drawing selection drawing 8



[Translation done.]